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REMARKS

Claims 1, 3, 5, 10, 12, 14, 20-22, and 24 have been amended. Claims 20-22 have had their punctuation and spacing changed to clarify that the programmable controller and memory unit are not part of the preamble of the claims. No new matter has been added.

35 U.S.C. §102

The examiner rejected claims 1, 4, 5, 8, and 25-44 under 35 U.S.C. § 102(e) as being anticipated by Lin '969. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. MPEP § 2131. Lin '969 does not anticipate claims 1, 4, 5, 8, or 25-44 because Lin '969 does not expressly or inherently describe each and every element as set forth in the claims.

For example, regarding amended claim 1, Lin '969 does not describe a single intermediate substrate positioned between a first semiconductor die and a second semiconductor die. Instead, Lin teaches a face to face a stacked integrated circuit assembly having more than one intermediate substrate. As seen in Fig. 3, Lin's integrated circuit assembly has two intermediate substrates 103-1, 103-2 facing each other between the integrated circuit chips 101-1, 101-2. Lin does not suggest using a single intermediate substrate located between the integrated circuit chips. Instead, Lin improves the speed of signal transmission by soldering solder balls 130-1, 130-2 of the intermediate substrates 103-1, 203-2 together (Col. 4, lines 41-46). Claims 25-43 are dependent on claim 1.

Regarding independent claim 4, Lin '969 does not teach, for example, a first semiconductor die electrically coupled to an intermediate substrate by at least one topographic contact extending from a first active surface to a first surface of an intermediate substrate. According to the specification, a topographic contact comprises any conductive contact that extends between and defines a spacing between an active surface of a substrate or die and an active surface of another substrate or die (Page 11, lines 22-24). Neither the first integrated circuit chip nor the second integrated circuit chip of Lin is electrically coupled to an intermediate substrate by at least one topographic contact. Instead, the integrated circuit chips 101-1, 101-2 are bonded to the intermediate substrate via an adhesive 102-1, 102-2. The integrated circuit chips 101-1, 101-2 are not electrically coupled via the adhesive 102-1, 102-2. Instead, bond wires 104"-1, 104"-2 extend through a window 104-1, 104-22 to electrically couple the

integrated circuit chips 101-1, 101-2 to the respective intermediate substrates 103-1, 103-2. Claim 44 is dependent on claim 4.

Regarding amended independent claim 5, Lin '969 does not teach, for example, an additional substrate positioned such that a first surface of an additional substrate faces a second active surface of a second semiconductor die and such that a first surface of an additional substrate opposes a second surface of an intermediate substrate. Instead, Lin '969 teaches an additional substrate to a 103-2 having a first surface that is electrically connected to and opposes a second intermediate substrate 103-1 and having an integrated circuit die 101-2 attached to a second surface of the additional substrate 103-2 as seen in Fig. 3. Additionally, Lin '969 does not suggest this arrangement because the intermediate substrates 103-1, 103-2 are not configured such that the second integrated circuit die 101-2 may be accommodated in a space between the intermediate substrates 103-1, 103-2. Instead, Lin '969 focuses on a face-to-face stacked integrated circuit assembly wherein the printed circuit boards 103-1, 103-2 are stacked face to face (Col. 4, lines 47-65).

Regarding independent claim 8, Lin '969 fails to teach, for example, a first semiconductor die electrically coupled to an intermediate substrate by at least one topographic contact extending from a first active surface of a first semiconductor die to a first surface of an intermediate substrate. Additionally, Lin '969 fails to teach a second semiconductor die electrically coupled to an intermediate substrate by at least one topographic contact extending from a second active surface of a second semiconductor die to a second surface of an intermediate substrate. As discussed above, Lin ' 969 does not teach topographic contacts electrically coupling the integrated circuit dies 101-1, 101-2 to the respective intermediate substrates 103-1, 103-2. Instead, Lin utilizes an adhesive 102-1, 102-2 to secure the integrated circuit dies and electrically couple the integrated circuit dies via bond wires 104"-1, 104"-2 to the respective intermediate substrates 103-1, 103-2. Therefore, claims 1, 4, 5, 8, and 25-44 are patentable over the cited and applied prior art.

35 U.S.C. § 103

The examiner rejected claims 2, 6, 7, 9, 45-48 under 35 U.S.C. § 103(a) as being unpatentable over Lin '969 in combination with Shoichi. According the Abstract, Shoichi relates to directly connecting the electrode of a semiconductor chip in a package with a capacitor.

Regarding claims 2, 6, 7, and 9, neither Lin '969 nor Shoichi teaches or suggests at least one decoupling capacitor conductively coupled to at least one of first and second semiconductor dies wherein a thickness dimension of a decoupling capacitor is accommodated in a space defined by a thickness dimension of one of the first semiconductor die, the second semiconductor die, a topographic contact conductively coupled to a first semiconductor die, and a topographic contact conductively coupled to a second semiconductor die.

As the examiner notes, Lin '969 does not show a decoupling capacitor. Shoichi does show a capacitor 10, but Shoichi does not show a thickness dimension of the capacitor accommodated in spaced defined by a thickness dimension of one of a first semiconductor die, a second semiconductor die, a topographic contact conductively coupled to a first semiconductor die, and a topographic contact conductively coupled to a second semiconductor die. Referring to Fig. 2a, a capacitor 10 is shown secured to an integrated circuit chip 2, but the thickness dimension of the capacitor 10 is not accommodated in a space defined by the integrated circuit chip 2. Instead, the integrated circuit chip 2 is stacked on top of capacitor 10. Referring to Fig. 3a, the capacitor 10 is shown mounted on a die stage 4 adjacent to the integrated circuit chip 2. Once again, the capacitor 10 is not accommodated in a thickness dimension defined by the integrated circuit chip 2 because the capacitor 10 is mounted on top of structure 28. Claims 45-48 are dependent on independent claim 6.

Additionally regarding claims 6 and 9, neither Lin '969 nor Shoichi teaches or suggests a first semiconductor die electrically coupled to an intermediate substrate by a at least one topographic contact extending from a first active surface of a first semiconductor die to a first surface of an intermediate substrate. As discussed above, Lin '969 does not suggest such topographic contacts. Shoichi does not show such contacts because the integrated circuit chip 2 is either shown directly coupled to die stage 4 or stacked on top of capacitor 10. Therefore, claims 2, 6, 7, 9, and 45-48 are patentable over the cited and applied prior art.

The examiner rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Lin '969 in combination with Shoichi and Toy. Toy relates to a cast metal seal for semiconductor substrates and shoes a semiconductor package having a cover 20 bonded to a heat sink 36.

Neither Lin, Shoichi, nor Toy teach or suggest a multiple die semiconductor assembly having a first semiconductor die, a second semiconductor die, and a single intermediate substrate positioned between a first semiconductor die and second semiconductor die. As discussed above,

Lin does not teach a single intermediate substrate positioned between a first semiconductor die and a second semiconductor die. Additionally, Lin does not suggest such a configuration because Lin's semiconductor package relates to the face-to-face stacked integrated circuit assembly wherein printed circuit boards are stacked face-to-face to improve packing density. The configurations of the present invention allow for denser packing than that suggested by Lin. Shoichi does not show a first and second semiconductor die. Referring to Fig. 1, Toy does not show an intermediate substrate position between a first semiconductor die and a second semiconductor die. Therefore, claim 3 is patentable over the cited and applied prior art.

The examiner rejected claims 10, 13, 14, 17, 20, 23, and 24 under 35 U.S.C. § 103(a) as being unpatentable over Lin '969 in view of Lin '23. Lin '423 relates to multi chip modules having a stacked configuration.

Regarding amended claims 10 and 20, neither Lin '969 nor Lin '423 teaches or suggests a single intermediate substrate defining an intermediate passage there through positioned between a first and second semiconductor die. As discussed above in conjunction with claims 1 and 3, Lin '969 does not teach or suggest a single intermediate substrate positioned between a first semiconductor die and a second semiconductor die. Lin '423 does not teach an intermediate substrate having a passage there through, and Lin does not teach a single intermediate substrate as can be seen in Figs. 2-5.

Regarding claims 13, 17, and 23, neither Lin '969 nor Lin '423 teaches or suggests a first semiconductor die electrically coupled to an intermediate substrate by at least one topographic contact extending from a first active surface of a first semiconductor die to a first surface of an intermediate substrate. As discussed above in conjunction with claims 4, 6, and 8, Lin '969 does not teach or suggest such contacts. As can be seen in Figs 2-5 of Lin '423, the semiconductor dies 24 are not bonded to the printed circuit boards 14 via topographic contacts.

Regarding amended claims 14 and 24, neither Lin '969 nor Lin '423 teaches or suggests an additional substrate defining a passage there through positioned such that a first surface of an additional substrate faces a second active surface of a second semiconductor die and such that a first surface of an additional substrate opposes a second surface of an intermediate substrate defining a passage there through. As discussed above in conjunction with claim 5, Lin ' 969 teaches an additional substrate having a first surface that is electrically connected to and opposes a second intermediate substrate and having an integrated circuit die attached to a second surface

of the additional substrate. Lin '969 does not suggest the arrangement of claims 14 and 24 as discussed above in conjunction with claim 5. Lin '423 does not teach or suggest such an arrangement. Lin '423 teaches semiconductor devices 11 having a semiconductor die 24 directly mounted to printed circuit boards 14. As can be seen in Figs. 2-5, the printed circuit boards 14 do not have intermediate passages defined there through. Therefore, claims 10, 13, 14, 17, 20, 23, and 24 are patentable over the cited and applied prior art.

The examiner rejected claims 11, 15, 16, 18, 21, and 49-53 under 35 U.S.C. § 103(a) as being unpatentable over Lin '969 and Lin '423 in combination with Shoichi. Regarding the rejected claims, neither Lin '969, Lin '423, nor Shoichi teaches or suggests at least one decoupling capacitor conductively coupled to at least one of a first and second semiconductor die, wherein a thickness dimension of a decoupling capacitor is accommodated in a space defined by a thickness dimension of a first semiconductor die, a second semiconductor die, a topographic contact conductively coupled to a first semiconductor die, and a topographic contact conductively coupled to a second semiconductor die. As discussed above in conjunction with claims 2, 6, 7, 9, and 45-48, neither Lin '969 nor Shoichi teaches or suggests a thickness dimension of a decoupling capacitor accommodated in a space defined by a thickness dimension of a first semiconductor die, a second semiconductor die, a topographic contact conductively coupled to a first semiconductor die, and a topographic contact conductively coupled to a second semiconductor die. As the examiner states, Lin '423 does not disclose a decoupling capacitor conductively coupled to a first or second semiconductor die. Therefore, claims 11, 15, 16, 18, 21, and 49-53 are patentable over the cited and applied prior art.

The examiner rejected claims 12, 19, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Lin '969 and Lin '423 in combination with Shoichi and Toy.

Regarding amended claims 12 and 22, neither Lin '969 or '423, Shoichi, nor Toy teach or suggest a multiple die semiconductor assembly having a first semiconductor die a, a second semiconductor die, and a single intermediate substrate defining a passage therethrough positioned between a first semiconductor die and second semiconductor die. As discussed above, Lin '969 and '423 do not teach a single intermediate substrate positioned between a first semiconductor die and a second semiconductor die. Additionally, Lin '969 does not suggest such a configuration because Lin's semiconductor package relates to the face-to-face stacked integrated circuit assembly wherein printed circuit boards are stacked face-to-face to improve

packing density. The configurations of the present invention allow for denser packing than that suggested by Lin '969. Lin '423 does not suggest an intermediate substrate defining a passage there through as discussed above. Shoichi does not show a first and second semiconductor die. Referring to Fig. 1, Toy does not show an intermediate substrate position between a first semiconductor die and a second semiconductor die.

Regarding claim 19, neither Lin '969, Lin '423, Shoichi, nor Toy teaches or suggests a semiconductor die electrically coupled to an intermediate substrate by at least one topographic contact extending from a first active surface to first surface of an intermediate substrate as discussed above. Therefore, claims 12, 19, and 22 are patentable over the cited and applied prior art.

CONCLUSION

Applicants respectfully submit that, in view of the above amendments and remarks, the application is now in condition for allowance. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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Appendix A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 1, 3, 5, 10, 12, 14, 20-22, and 24 have been amended.

1. (Amended) A multiple die semiconductor assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad; and

~~an~~ a single intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first semiconductor die and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through, and

one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage.

3. (Amended) A multiple die semiconductor assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

~~an~~ a single intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first semiconductor die and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through, and

one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage; and

a heat sink including a cap portion and a peripheral portion, wherein

said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor dies, and

said peripheral portion engages a mounting zone defined by a lateral dimension of said intermediate substrate extending beyond a periphery of at least one of said first and second semiconductor dies.

5. (Amended) A multiple die semiconductor assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate positioned between said second semiconductor die and said first active surface of said first semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through,

said first semiconductor die is secured to said first surface of said intermediate substrate such that said conductive bond pad of said first semiconductor die is aligned with said passage, and

said first semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said first semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said second surface of said intermediate substrate; and

an additional substrate positioned such that a first surface of said additional substrate faces said second active surface of said second semiconductor die and such that said first surface of said additional substrate opposes said second surface of said intermediate substrate, wherein

said additional substrate defines an additional passage there through,

said second semiconductor die is secured to said first surface of said additional substrate such that said conductive bond pad of said second semiconductor die is aligned with said additional passage, and

said second semiconductor die is electrically coupled to said additional substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said additional passage defined in said additional substrate and to a conductive contact on a second surface of said additional substrate.

10. (Amended) A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

~~an~~ a single intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first semiconductor die and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through, and

one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage;

a printed circuit board positioned such that a first surface of said printed circuit board faces said intermediate substrate; and

a plurality of topographic contacts extending from said intermediate substrate to said first surface of said printed circuit board.

12. (Amended) A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

~~an~~ a single intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first semiconductor die and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through, and

one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage;

a printed circuit board positioned such that a first surface of said printed circuit board faces said intermediate substrate;

a plurality of topographic contacts extending from said intermediate substrate to said first surface of said printed circuit board; and

a heat sink including a cap portion and a peripheral portion, wherein

said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor dies, and

said peripheral portion engages a mounting zone defined by a lateral dimension of said intermediate substrate extending beyond a periphery of at least one of said first and second semiconductor dies.

14. (Amended) A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate positioned between said second semiconductor die and said first active surface of said first semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through,

said first semiconductor die is secured to said first surface of said intermediate substrate such that said conductive bond pad of said first semiconductor die is aligned with said passage, and

said first semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said first semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said second surface of said intermediate substrate;

an additional substrate positioned such that a first surface of said additional substrate faces said second active surface of said second semiconductor die and such that said first surface of said additional substrate opposes said second surface of said intermediate substrate, wherein

said additional substrate defines an additional passage there through,

said second semiconductor die is secured to said first surface of said additional substrate such that said conductive bond pad of said second semiconductor die is aligned with said additional passage, and

said second semiconductor die is electrically coupled to said additional substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said additional passage defined in said additional substrate and to a conductive contact on a second surface of said additional substrate;

a printed circuit board positioned such that a first surface of said printed circuit board faces said second surface of said additional substrate and such that said conductive line extends through a space defined between said second surface of said additional substrate and said first surface of said printed circuit board; and

a plurality of topographic contacts extending from said second surface of said additional substrate to said first surface of said printed circuit board.

20. (Amended) A computer system comprising:

-a programmable controller; and

at least one memory unit, wherein said memory unit comprises a printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

———a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

———~~an~~a single intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first semiconductor die and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

———said intermediate substrate defines a passage there through, and

———one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage;

———a printed circuit board positioned such that a first surface of said printed circuit board faces said intermediate substrate; and

———a plurality of topographic contacts extending from said intermediate substrate to said first surface of said printed circuit board.

21. (Amended) A computer system comprising:

a programmable controller; and

at least one memory unit, wherein said memory unit comprises a printed circuit board assembly comprising:

———a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

———a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

———an intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first semiconductor die and such that a

second surface of said intermediate substrate faces said second semiconductor die, wherein

———said intermediate substrate defines a passage there through, and

———one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage;

———a printed circuit board positioned such that a first surface of said printed circuit board faces said intermediate substrate;

———a plurality of topographic contacts extending from said intermediate substrate to said first surface of said printed circuit board; and

———at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of

———said first semiconductor die,

———said second semiconductor die,

———a topographic contact conductively coupled to said first semiconductor die, and

———a topographic contact conductively coupled to said second semiconductor die.

22. (Amended) A computer system comprising:

a programmable controller; and

at least one memory unit, wherein said memory unit comprises a printed circuit board assembly comprising:

———a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

———a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

——~~an~~ a single intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first semiconductor die and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

——said intermediate substrate defines a passage there through, and

——one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage;

——a printed circuit board positioned such that a first surface of said printed circuit board faces said intermediate substrate;

——a plurality of topographic contacts extending from said intermediate substrate to said first surface of said printed circuit board; and

a heat sink including a cap portion and a peripheral portion, wherein

——said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor dies, and

——said peripheral portion engages a mounting zone defined by a lateral dimension of said intermediate substrate extending beyond a periphery of at least one of said first and second semiconductor dies.

24. (Amended) A method of stacking a plurality of semiconductor die comprising:

providing a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

providing a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

positioning an intermediate substrate between said second semiconductor die and said first active surface of said first semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second semiconductor die;

securing said first semiconductor die to said first surface of said intermediate substrate such that said conductive bond pad of said first semiconductor die is aligned with a passage formed in said intermediate substrate;

electrically coupling said first semiconductor die to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said first semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said second surface of said intermediate substrate;

providing an additional substrate positioned such that a first surface of said additional substrate faces said second active surface of said second semiconductor die and such that said first surface of said additional substrate opposes said second surface of said intermediate substrate;

securing said second semiconductor die to said first surface of said additional substrate such that said conductive bond pad of said second semiconductor die is aligned with an additional passage formed in said additional substrate;

electrically coupling said second semiconductor die to said additional substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said additional passage defined in said additional substrate and to a conductive contact on a second surface of said additional substrate;

positioning a printed circuit board such that a first surface of said printed circuit board faces said second surface of said additional substrate and such that said conductive line extends through a space defined between said second surface of said additional substrate and said first surface of said printed circuit board; and

forming a plurality of topographic contacts extending from said second surface of said additional substrate to said first surface of said printed circuit board.